WHAT IS CLAIMED IS

1. An apparatus for measuring a clock skew between a plurality of clock signals under measurement comprising:

a timing jitter estimator to which the plurality of clock signals under measurement are inputted for estimating their respective timing jitter sequences; and

a clock skew estimator to which the plurality of timing jitter sequences are inputted for calculating a timing difference sequence between those timing jitter sequences to output a clock skew sequence.

2. The apparatus for measuring a clock skew between a plurality of clock signals under measurement according to claim 1 further including:

a second clock skew estimator to which a plurality of the clock skew sequences are inputted for obtaining a difference between the plurality of clock skew sequences.

3 The apparatus for measuring a clock skew between a plurality of clock signals under measurement according to claim 2 further including:

a frequency multiplier to which the timing jitter sequence is inputted for multiplying a frequency of the timing jitter sequence to output the frequency-multiplied timing jitter sequence to said clock skew estimator.

4 The apparatus for measuring a clock skew between a plurality of clock signals under measurement according to claim 1 further including:

a frequency multiplier to which the timing jitter sequence is inputted

for multiplying a frequency of the timing jitter sequence to output the frequency-multiplied timing jitter sequence to said clock skew estimator.

5. The apparatus for measuring a clock skew between a plurality of clock signals under measurement according to claim 1 further including a deterministic clock skew estimator for estimating a timing error between ideal clock edges of the plurality of clock signals under measurement to output a deterministic component of clock skew to said clock skew estimator, wherein said clock skew estimator is an estimator for adding the deterministic component of clock skew to the timing difference sequence to output the summed value as the clock skew sequence.

6. The apparatus for measuring a clock skew between a plurality of clock signals under measurement according to any one of claims 1-5 further including:

a clock skew detector to which the clock skew sequence is inputted for obtaining clock skew values of the clock signals under measurement from the clock skew sequence.

7. The apparatus for measuring a clock skew between a plurality of clock signals under measurement according to claim 6, wherein said clock skew detector comprises one or a plurality of a peak-to-peak detector for obtaining a difference between the maximum value and the minimum value of the clock skew sequence, an RMS detector for obtaining a root-mean-square value of the clock skew sequence, and a histogram

estimator for obtaining a histogram of the clock skew sequence.

8. The apparatus for measuring a clock skew between a plurality of clock signals under measurement according to any one of claims 1-5, wherein said timing jitter estimator comprises;

an analytic signal transformer for transforming a clock signal under measurement into a complex analytic signal;

an instantaneous phase estimator for obtaining an instantaneous phase of the analytic signal;

a continuous phase converter for converting the instantaneous phase into a continuous instantaneous phase;

a linear phase estimator for estimating, from the continuous instantaneous phase, its linear instantaneous phase;

a subtractor for removing the linear instantaneous phase from the continuous instantaneous phase to obtain an instantaneous phase noise; and

a zero-crossing sampler for sampling its input at timings close to zero-crossing timings of a real part of the analytic signal to output the sampled signal, said zero-crossing sampler being inserted in series to any one of connection points between said instantaneous phase estimator and said continuous phase converter, between said continuous phase converter and said linear phase estimator/subtractor, and at an output side of said subtractor;

wherein a timing jitter sequence of the clock signal under measurement is outputted as an output of said timing jitter estimator.

9. The apparatus for measuring a clock skew between a plurality of clock signals under measurement according to claim 8, wherein said deterministic clock skew estimator of the plurality of clock signals under measurement is an estimator that obtains a difference between initial phase angles of the linear instantaneous phases to obtain a deterministic component of clock skew.

10. The apparatus for measuring a clock skew between a plurality of clock signals under measurement according to claim 8, wherein said analytic signal transformer can change a pass bandwidth of the clock signal under measurement.

11. The apparatus for measuring a clock skew between a plurality of clock signals under measurement according to claim 8, wherein said timing jitter estimator includes a low frequency component remover to which the instantaneous phase noise is inputted for removing low frequency components of the instantaneous phase noise to output the instantaneous phase noise from which the low frequency components have been removed.

12. The apparatus for measuring a clock skew between a plurality of clock signals under measurement according to any one of claims 1-5 further including;

a waveform clipper to which the clock signal under measurement is inputted for removing amplitude modulation components of the clock signal under measurement in the state that phase modulation components are

retained in the clock signal under measurement to output the clock signal under measurement from which the amplitude modulation components have been removed.

13. A method of measuring a clock skew between a plurality of clock signals under measurement comprising:

a step of estimating timing jitter sequences of the respective clock signals under measurement; and

a step of calculating a timing difference sequence between the plurality of timing jitter sequences to estimate a clock skew sequence.

14. The method of measuring a clock skew between a plurality of clock signals under measurement according to claim 13 further including:

a step of obtaining a difference between the plurality of clock skew sequences to estimate a clock skew sequence.

15. The method of measuring a clock skew between a plurality of clock signals under measurement according to claim 14 further including:

a step of assign each timing jitter of the timing jitter sequence M times to estimate a timing jitter sequence that is created by multiplying a frequency of the corresponding clock signal under measurement by (M+1).

16. The method of measuring a clock skew between a plurality of clock signals under measurement according to claim 13 further including:

a step of assign each timing jitter of the timing jitter sequence M times to estimate a timing jitter sequence that is created by multiplying a

frequency of the corresponding clock signal under measurement by (M+1).

17. The method of measuring a clock skew between a plurality of clock signals under measurement according to claim 13 further including a step of estimating a timing error between ideal clock edges of the plurality of clock signals under measurement to estimate a deterministic component of clock skew, wherein said step of estimating a clock skew sequence is a step of adding the deterministic component of clock skew to the timing difference sequence to obtain the summed value as the clock skew sequence.

18. The method of measuring a clock skew between a plurality of clock signals under measurement according to any one of claims 13-17 further including:

a step of obtaining clock skew values of the clock signals under measurement from the clock skew sequence.

19. The method of measuring a clock skew between a plurality of clock signals under measurement according to claim 18, wherein said step of obtaining a clock skew comprises one or a plurality of a step of obtaining a difference between the maximum value and the minimum value of the clock skew sequence to calculate a peak-to-peak value, a step of obtaining a root-mean-square value of the clock skew sequence to calculate an RMS value, and a step of obtaining a histogram data of the clock skew sequence.

20. The method of measuring a clock skew between a plurality of clock

signals under measurement according to any one of claims 13-17, wherein said step of estimating a timing jitter sequence comprises;

a step of transforming a clock signal under measurement into a complex analytic signal;

a step of obtaining an instantaneous phase of the clock signal under measurement from the analytic signal;

a step of converting the instantaneous phase into a continuous instantaneous phase;

a step of estimating, from the continuous instantaneous phase, its linear instantaneous phase;

a step of removing the linear instantaneous phase from the continuous instantaneous phase to obtain an instantaneous phase noise; and

a step of sampling any one of the instantaneous phase, the continuous instantaneous phase, and the phase noise waveform at timings close to zero-crossing timings of a real part of the analytic signal,

wherein a timing jitter sequence of the clock signal under measurement is eventually obtained.

21. The method of measuring a clock skew between a plurality of clock signals under measurement according to claim 20, wherein said step of estimating a deterministic component of clock skew between the clock signals under measurement is a step of obtaining a difference between initial phase angles of linear instantaneous phases of the plurality of clock signals under measurement to obtain a deterministic component of clock skew.

22. The method of measuring a clock skew between a plurality of clock signals under measurement according to claim 21, wherein said step of estimating a deterministic component of clock skew between the clock signals under measurement comprises:

a step of obtaining an offset signal in which either a correlation between timing jitter sequences of the plurality of clock signals under measurement or a correlation between instantaneous phase noises of the plurality of clock signals under measurement shows the maximum value to obtain an offset value of clock edge; and

a step of obtaining a sum of the offset value and the difference between the initial phase angles to obtain the deterministic component of clock skew.

23. The method of measuring a clock skew between a plurality of clock signals under measurement according to claim 20, wherein said step of estimating a deterministic component of clock skew between the clock signals under measurement is a step of obtaining a mean value of differences of zero-crossing timings between the plurality of signals under measurement to obtain a deterministic component of clock skew.

24. The method of measuring a clock skew between a plurality of clock signals under measurement according to claim 20, wherein said step of estimating a timing jitter includes a step of removing low frequency components of the instantaneous phase noise.

25. The method of measuring a clock skew between a plurality of clock signals under measurement according to any one of claims 13-17 further including;

a step of performing a waveform clipping in the state that phase modulation components of the clock signal under measurement are retained to remove amplitude modulation components of the clock signal under measurement, and moving to the step of estimating a timing jitter sequence.